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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech I Year II Semester Supplementary Examinations May-2022

DIGITAL LOGIC DESIGN

(Common to CSE, CSIT, CSM & CIC)

Time: 3 hours

Max. Marks:60

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

- 1 a i)(41.6875)₁₀ to Hexadecimal number L5 6M
 ii)(11001101.0101)₂ to base-8 and base-4
 b Subtract (111001)₂ from (101011) using 2's complement. L5 6M
- OR**
- 2 a Express the Boolean function $F=A+B^1 C$ as a sum of min terms. L1 6M
 b Convert the given expression in standard POS form: $Y=A(A+B+C)$. L6 6M

UNIT-II

- 3 Simplify the following Boolean expression using K-MAP and implement using NAND gates. $F(W,X,Y,Z)=XYZ+WXY+WYZ+WXZ$ L6 12M
- OR**
- 4 a Design the circuit by Using NAND gates L6 6M
 $F= ABC'+DE+AB'D'$
 b Design the circuit by Using NOR gates L6 6M
 $F= (X+Y).(X'+Y'+Z')$

UNIT-III

- 5 Draw and explain the working of a Carry- Look ahead adder. L2 12M
- OR**
- 6 a What is combinational circuits and explain analysis and design procedure of combinational circuits. L1 6M
 b Explain about Priority encoder. L2 6M

UNIT-IV

- 7 a Explain the Logic diagram of JK flip-flop. L2 6M
 b Write difference between Combinational & Sequential circuits. L5 6M
- OR**
- 8 Explain the design of a 4 bit binary counter with parallel load in detail. L2 12M

UNIT-V

- 9 Explain about Error correction & Detection Codes with examples. L2 12M
- OR**
- 10 Implement the following functions using PLA L5 12M
 $A(x,y,z)=\sum m(1,2,4,6)$, $B(x,y,z)=\sum m(0,1,6,7)$, $C(x,y,z)=\sum m(2,6)$

*** END ***